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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,185	07/31/2003	Gerard Chauvel	TI-35431 (1962-05410)	1444

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EXAMINER	
SAVLA, ARPAN P	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,185	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,10-14 and 17-20* is/are rejected.

7)☒ Claim(s) *7,9,15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/31/03, 4/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/631185 has a total of 20 claims pending in the application, there are 3 independent claims and 17 dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Receipt is acknowledged of papers filed under 35 U.S.C. 119 (a)-(d) based on an application filed in the European Patent Office on July 30, 2003. Applicant has not complied with the requirements of 37 CFR 1.63(c), since the oath does not acknowledge the filing of any foreign application. A new oath is required in the body of which the present application should be identified by application number and filing date.

STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

2. As required by MPEP § 201.14(c), acknowledgment is made of Applicant's claim for priority based on an application filed in the European Patent Office on July 30th, 2003. Acknowledgment is also made of Applicant's claim for priority based on a U.S. provisional application filed July 31st, 2002.

INFORMATION CONCERNING DRAWINGS

Drawings

3. Applicant's drawings submitted are acceptable for examination purposes.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

4. As required by MPEP § 609(c), Applicant's submission of both Information Disclosure Statements dated July 30, 2003 and April 12, 2004 are acknowledged by Examiner and cited references have been considered in the examination of the claims now pending. As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by Examiner is attached to the instant office action.

OBJECTIONS

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Dirty Cache Line Write Back Policy Based On Stack Size Trend Information".

6. The disclosure is objected to because of the following informalities:

7. In paragraph 0001 and subsequent paragraphs Applicant must properly identify all co-pending applications with their corresponding application numbers (i.e. serial numbers).

8. In paragraph 0019, line 4 the phrase "a upper portion" should be "an upper portion".

9. In paragraph 0021, the last line of the paragraph needs a period at the end of the sentence.

10. In paragraph 0023, line 19 the phrase "FUTURE 70 represents signal" should be "FUTURE 70 represents a signal".

11. The phrases "decode logic", "decoder logic", and "decoder" are all interchangeably used to describe element 20 in the figures. Applicant must choose only one phrase to describe element 20 and then consistently use that phrase to refer to element 20 throughout the specification.

Appropriate corrections are required.

Claims

12. Claims 12-15, and 20 are objected to because of the following informalities:

13. **As per claim 12-14**, the phrases "decoder" and "decode logic" are interchangeably used to describe element 20 in the figures. Applicant must choose only one phrase to describe element 20 and then consistently use that phrase to refer to element 20 throughout the claims.

14. **Also for claim 14**, the word "potion" in line 1 should be "portion".

15. **As per claim 15**, the claim recites the limitation "the cache memory" in line 1. There is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending this claim to read "cache memory" in line 1.

16. **As per claim 20**, the phrase "the stack size decreasing" should be "the stack size is decreasing".

Appropriate corrections are required.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

18. Claims 1-4, 8, 11, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Shen et al. (U.S. Patent 5,687,336).

19. As per claim 1, Shen discloses a method of managing memory, comprising:

examining current and future instructions operating on a stack (col. 3, line 65 col. 7, line 7 and Fig. 2);

determining stack trend information (col. 4, lines 11-15 and 36-60; and Fig. 2); It should be noted that Shen's final value for the stack pointer indicates whether the stack size has increased or decreased.

utilizing the trend information to reduce data traffic between various levels of a memory (col. 2, lines 24-27). It should be noted that executing multiple stack instructions simultaneously reduces data traffic and that stack registers are a form of memory.

20. **As per claim 2**, Shen discloses determining the trend information includes examining future instructions to determine if the size of the stack is going to decrease as a result of future instructions (col. 3, line 65 – col. 7, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-5 and 9-10; and Fig. 2).

21. **As per claim 3**, Shen discloses a predetermined number of instructions are used in determining stack trend information (col. 3, lines 65-67 and col. 6, lines 47-48). It should be noted that if there is only one instruction per stage and there are five stages in the pipeline, then five instructions are used in determining stack trend information.

22. **As per claim 4**, Shen discloses the number of predetermined instructions is at least two (col. 3, lines 65-67 and col. 6, lines 47-48). See citation note for claim 3 above.

23. **As per claim 8**, Shen discloses determining the trend information includes examining future instructions to determine if the size of the stack is going to increase as a result of future instructions (col. 3, line 65 – col. 7, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-7; and Fig. 2).

24. **As per claim 11**, Shen discloses a computer system, comprising:

a processor (col. 4, line 37 and Fig. 2);

a memory coupled to the processor (col. 4, lines 33-34 and Fig. 2, element 26); It should be noted that the memory physically lies within the processor, thus making the memory and processor coupled.

a stack that exists in memory and contains stack data (col. 4, lines 33-34 and Fig. 2, element 26);

a memory controller coupled to the memory (col. 5, lines 19-23). It should be noted that Shen does not expressly disclose a memory controller in the design. However, the citation noted above discloses reading from and writing to a cache memory. As one of ordinary skill in the art knows a memory controller is inherently required to interface with any memory.

trend logic (col. 4, lines 40-43 and Fig. 2, element 20);

wherein the processor executes instructions (col. 4, lines 36-37);

wherein the trend logic provides trend information about the stack to the controller (col. 5, lines 10-14 and 19-22; Fig. 2, elements 20, 24, 40, and 94); It should noted that the trend information is calculated by the three-way addition of the stack pointer, segment base, and increment value (which comes from the increment logic) and then the trend information is sent from the three-port adder to the memory controller.

wherein the trend information about the stack is based on at least one future instruction (col. 3, line 65 – col. 7, line 7; col. 4, lines 11-15 and 36-60; and Fig. 2).

25. **As per claim 13**, Shen discloses the trend logic determines a net stack trend based on current instruction and future instruction information coming from the decode logic (col. 3, line 65 – col. 7, line 7; col. 4, lines 11-15; col. 4, lines 36-60; and Fig. 2, elements 20, 30, and 94).

26. Claim 18 is rejected under 35 U.S.C. 102(e) as being anticipated by Steely et al. (U.S. Patent 6,801,986).

27. Steely discloses the method of claim 17, further comprising determining whether the write request will be to the end of a dirty cache line (col. 8, lines 55-57 and Fig. 2A, element 221). It should be noted that when taking the broadest interpretation of the claim language it is clear that the limitations of the claim do not specify how many words are in a dirty cache line. Steely does not disclose the exact size of a cache line, however, at minimum it must contain one word, meaning a write request would always write bits to both the beginning and end of a dirty cache line.

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claim 5 is rejected under 35 U.S.C. 103(a) as being obvious over Shen et al. in view of Ebrahim et al. (U.S. Patent 5,893,121).

30. Shen discloses the method of claim 1.

31. Shen does not disclose expressly the cache memory maintains a single dirty cache line for stack data.

Ebrahim discloses the cache memory maintains a single dirty cache line for stack data (col. 5, lines 32-35). It should be noted that a cache block maintaining a dirty bit is analogous to a "dirty cache line".

Shen and Ebrahim are analogous art because they are from the same field of endeavor, that being stack memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Ebrahim's stack cache memory containing a single dirty cache line within Shen's stack trend tracker system.

The motivation for doing so would have been to avoid writing back unmodified stack cache blocks to main memory (Ebrahim, col. 5, lines 33-35).

Therefore, it would have been obvious to combine Ebrahim with Shen for the benefit of obtaining the invention as specified in claim 5.

32. Claims 6 and 10 are rejected under 35 U.S.C. 103(a) as being obvious over Shen et al. in view of Steely et al.

33. **As per claim 6**, Shen discloses the method of claim 3.

Shen does not disclose expressly determining which word of the dirty cache line is going to be written to.

Steely discloses determining which word of the dirty cache line is going to be written to (col. 2, lines 39-43). It should be noted that when taking the broadest interpretation of the claim language it is clear that the limitations of the claim do not specify how many words are in a dirty cache line. Steely does not disclose the exact size of a cache line, however, at minimum it must contain one word, meaning a write request would always go to a predetermined word with a dirty cache line, that being the only word in the dirty cache line.

Shen and Steely are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Steely's dirty cache line write procedure with Shen's stack trend tracker system.

The motivation for doing so would have been to produce an atomic read/write sequence which reduces the number of system commands and so reduces system overhead during contention for a memory block by two or more processors in a multiprocessor computer system (Steely, col. 6, lines 14-18). See col. 2, lines 46-49 for a definition of an "atomic read/write".

Therefore, it would have been obvious to combine Steely with Shen for the benefit of obtaining the invention as specified in claim 6.

34. **As per claim 10**, Steely discloses the dirty cache line is written from a cache memory to a main memory (col. 9, lines 63-65; Fig. 1, elements 108 and 116; and Fig. 2A, element 221).

35. Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being obvious over Shen et al. in view of O'Connor et al. (U.S. Patent 6,026,485).

36. **As per claim 12**, Shen discloses the computer system of claim 11.

Shen does not disclose expressly an instruction decoder comprising a first portion that decodes current instructions and a second portion that decodes future instructions.

O'Connor discloses an instruction decoder comprising a first portion that decodes current instructions and a second portion that decodes future instructions (col. 3, lines

5-10; col. 3, lines 15-18; col. 3, lines 42-48). It should be noted that first instructions are current instructions while second instructions are future instructions.

Shen and O'Connor are analogous art because they are from the same field of endeavor, that being stack-based instruction processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use O'Connor's instruction decoder within Shen's stack trend tracker system.

The motivation for doing so would have been to identify foldable instruction sequences and supply an execution unit with an equivalent folded operation thereby reduce processing cycles otherwise required for decoding and executing multiple operations corresponding to the multiple instructions of the folded instruction sequence (O'Connor, col. 3, lines 20-25).

Therefore, it would have been obvious to combine O'Connor with Shen for the benefit of obtaining the invention as specified in claim 12.

37. **As per claim 14**, O'Connor discloses the second portion of the decoder is adjusted so that the number of future instructions that are decoded equals at least two (col. 3, lines 59-60). It should be noted that first instructions are current instructions while second and third instructions are both future instructions.

38. Claims 17 and 19-20 are rejected under 35 U.S.C. 103(a) as being obvious over Steely et al. in view of Shen et al.

39. **As per claim 17**, Steely discloses a method, comprising:

issuing a write request to a cache memory, wherein the cache memory includes multiple cache lines (col. 1, lines 51-52, col. 9, lines 61-62; and Fig. 2A, element 221); It should be noted that the presence of probe commands and cache tags indicate the cache memory has multiple cache lines.

determining whether the write request refers to a predetermined word within a dirty cache line (col. 2, lines 39-43); It should be noted that when taking the broadest interpretation of the claim language it is clear that the limitations of the claim do not specify how many words are in a dirty cache line. Steely does not disclose the exact size of a cache line, however, at minimum it must contain one word, meaning a write request would always go to a predetermined word with a dirty cache line, that being the only word in the dirty cache line.

Steely does not disclose expressly a method, comprising:

determining whether the size of a stack is increasing or decreasing.

Shen discloses a method, comprising:

determining whether the size of a stack is increasing or decreasing (col. 3, line 65 – col. 7, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-7 and 9-10; and Fig. 2).

Steely and Shen are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Shen's stack size tracker system with Steely's write-back policy.

The motivation for doing so would have been to use stack size information for the purposes of generating the stack pointer at the end of the pipeline, thus reducing

pipeline stalls produced by future instructions waiting for an updated stack pointer (Shen, col. 2, lines 5-11).

Therefore, it would have been obvious to combine Shen with Steely for the benefit of obtaining the invention as specified in claim 17.

40. **As per claim 19**, Steely discloses the dirty cache line is written to main memory (col. 9, lines 63-65; Fig. 1, elements 108 and 116; and Fig. 2A, element 221).

Steely does not disclose expressly the stack size is increasing.

Shen discloses the stack size is increasing (col. 5, lines 5-7).

41. **As per claim 20**, Steely discloses the method of claim 18, wherein the dirty cache line is retained in the cache memory (col. 9, lines 63-67; Fig. 1, elements 108 and 116; and Fig. 2A, element 221). It should be noted that when taking the broadest interpretation of the claim language it is clear that the limitations of the claim do not specify how much time elapses before a dirty cache line is written back to main memory (i.e. how long the dirty cache is retained in cache memory). Steely discloses that the dirty cache line will be written back into main memory at some point in time.

Steely does not disclose expressly the method of claim 18, wherein the stack size is decreasing.

Shen discloses the method of claim 18, wherein the stack size is decreasing (col. 5, lines 9-10).

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

The following references disclose various uses of **stack cache memory**.

U.S. Patent Number

4,928,239

5,893,148

6,151,661

6,209,061

6,671,196

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

a. **SUBJECT MATTER CONSDIERED ALLOWABLE**

Claims 7, 9, and 15-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reason for allowance of **claims 7 and 15** in the instant application is the recitation of "the trend information is used to restrict writing dirty cache lines from cache memory to main memory when the trend information indicates the stack size is

decreasing." **As per claim 9**, the recitation of "determining if a line is written back includes analyzing the trend information and includes examining a dirty cache line to determine which word of the dirty cache line is going to be written to." **As per claim 16**, the recitation of "the dirty cache line is written to main memory if the trend information indicates the stack is increasing."

b. **CLAIMS REJECTED IN THE APPLICATION**

Per the instant office action, **claims 1-6, 8, 10-14, and 17-20** have received a first action on the merits and are subject of a first action non-final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arpan P. Savla
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11/14/05

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SUPERVISORY PATENT EXAMINER